REMARKS

Applicant has amended the specification to comply with the provisions of 35 U.S.C. 120. As such, this amendment does not constitute new matter and its entry is respectfully requested.

Claims 3, 5, 9, 10, 12, 13, 16 and 17 have been amended to remove multiple-dependent claims. No new matter has been added by virtue of the amendments to the claims and the addition of new claims. A copy of the Version with Markings to Show Changes Made to Claims is submitted herewith.

In view of the foregoing amendment it is respectfully submitted that all claims are in condition for allowance. Early and favorable action is requested.

If any additional fee is required, charge Deposit Account No. 50-0850.

Date: 1 August 2001

Respectfully submitted,

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MARKDED VERSION TO SHOW CHANGES MADE TO CLAIMS

CLAIMS

1. A neural processing element (100) for use in a neural network, the processing element comprising:

arithmetic logic means (50);

an arithmetic shifter mechanism (52);

data multiplexing means (115,125);

memory means (56,57, 58, 59);

data input means (110) including at least one input port;

data output means (120) including at least one output port; and

control logic means (54).

2. A neural processing element (100) as claimed in Claim 1, wherein each neural processing element (100) is a single neuron in the neural network.

3. (amended) A processing element as claimed in Claim 1 [or 2], further including data bit-size indicator means.

4. A processing element as claimed Claim 3, wherein the data bit-size indicator means enables operations on different bit-size data values to be executed using the same instruction set.

5. (amended) A processing element as claimed in [any one preceding claim] Claim 1, further including at least one register means.

6. A processing element as claimed in Claim 5, wherein the register means operates on different

bit-size data in accordance with said data bit-size indicator means.

7. A neural network controller (200) for controlling the operation of at least one processing element (100) as claimed in any one of claims 1 to 6, the controller (200) comprising

control logic means(270,280);

data input means (60) including at least one input port;

data output means (62) including at least one output port;

data multiplexing means (290, 292, 294);

memory means(64,68,280);

an address map (66);and

at least one handshake mechanism (210,220,230).

8. A neural network controller as claimed in Claim 7, wherein the memory means includes programmable memory means.

9. (amended) A neural network controller as claimed in Claim 7 [or 8], wherein the memory means includes buffer memory associated with said data input means and/or said data output means.

10. (amended) A neural network module (300) comprising an array of neural processing elements (100) as claimed in [any one of Claim 1 to 6] Claim 1; and at least one neural network controller (200) as claimed in [any one of claims 7 to 9] Claim 7.

11. A module (300) as claimed in claim 10, wherein the number of processing elements (100) in the array is a power of two.

12. (amended) A modular neural network comprising:
one module (300) as claimed in [either claim 10 or 11] Claim 10, or at least two modules (300) as claimed in [either claim 10 or 11] Claim 10 coupled together.

13. (amended) A modular neural network as claimed in [claim 14] Claim 12, wherein the modules (300) are coupled in a lateral expansion mode and/or a hierarchical mode.

14. A modular neural network as claimed in claim 12, including synchronisation means to facilitate data input to the neural network.

15. A modular neural network as claimed in claim 14, wherein said synchronisation means enables data to be input only once when the modules (300) are coupled in hierarchical mode.

16. A modular neural network as claimed in [either] claim 14 [or claim 15], wherein the synchronisation means includes the use of a two-line handshake mechanism.

17. (amended) A neural network device comprising a neural network as claimed in [any one of Claims 12 to 16] Claim 12, wherein an array of processing elements (100) is implemented on the neural network device with at least one module controller (200).

18. A device as claimed in claim 17, wherein the device is a field programmable gate array (FPGA) device.

19. A device as claimed in claim 17, comprising one of the following: a full-custom very large scale integration (VLSI) device, a semi-custom VLSI device, or an application specific integrated circuit (ASIC) device.

20. A method of training a neural network comprising the steps of:

providing a network of neurons (100), wherein each neuron(100) is reads an input vector applied to the input of the neural network;

enabling each neuron (100)to calculate its distance between the input vector and a reference vector according to a predetermined distance metric, wherein the neuron (100)with the minimum distance between its reference vector and the current input becomes the active neuron (100a);

outputting the location of the active neuron(100a); and

updating the reference vectors for all neurons (100) located within a neighbourhood around the active neuron (100a).

21. A method as claimed in Claim 20, wherein the predetermined distance metric is the Manhattan distance metric.

22. A method as claimed in Claim 21, wherein each neuron (100) of the neural network updates its reference vector if it is located within a step-function neighbourhood.

23. A method as claimed in Claim 22, wherein the step-function neighbourhood is a square function neighbourhood rotated by 45°.